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Direct Patterning of Self-Assembled Monolayers by Stamp Printing Method and Applications in High Performance Organic Field-Effect Transistors and Complementary Inverters

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Self-assembled monolayer (SAM) is usually applied to tune the interface between dielectric and active layer of organic field-effect transistors (OFETs) and other organic electronics, a time-saving, direct patterning approach of depositing well-ordered SAMs is highly desired. Here, a new direct patterning method of SAMs by stamp printing or roller printing with special designed stamps is introduced. The chemical structures of the paraffin hydrocarbon molecules and the tail groups of SAMs have allowed to use their attractive van der Waals force for the direct patterning of SAMs. Different SAMs including alkyl and fluoroalkyl silanes or phosphonic acids are used to stamp onto different dielectric surfaces and are characterized by water contact angle, atomic force microscopy, X-ray diffraction, and attenuated total reflectance Fourier transform infrared. The p-type dinaphtho[2,3-b:2′,3′-f]thieno[3,2-b]-thiophene (DNTT) and n-type $F_{16}CuPc$ OFETs show competitive mobility as high as 3 and 0.018 $cm^2 V^{-1} s^{-1}$, respectively. This stamp printing method also allows to deposit different SAMs on certain regions of same substrate, and the complementary inverter consists of both p-type and n-type transistors whose threshold voltages are tuned by stamp printing SAMs and shows a gain higher than 100. The proposed stamp or roller printing method can significantly reduce the deposition time and compatible with the roll-to-roll fabrication.

1. Introduction

Organic field-effect transistor (OFET) is a key electronic device which has applications that cover a wide range of areas, such as for use in display drivers, sensors, integrated circuits, and a lot more.[1–4] In the OFETs, the quality of the interface between the dielectric insulator and active layer is directly correlated to the performance parameters of the device, such as operating frequency, on/off ratio, subthreshold swing, and carrier mobility. To investigate such surface effect of the dielectric layers of OFETs, we have recently studied the mechanisms to modify the surface energy of barium strontium titanate (BST) high-k dielectric by varying the exposure environment and duration, and more importantly, its relationship with the growth mode of organic semiconductor (OSC) thin films and the overall device performance.[5] In general, the growth of OSC thin films can be divided into three different modes, Volmer–Weber (small island), Frank–van der Merwe (layer-by-layer), or Stranski–Krastanov (layer plus island). The different modes would result in distinctive grain size or boundary density which would govern the carrier mobility of OFETs. The growth condition is particularly important for the first few nanometers of the organic film because the conductive channels developed under gate bias are always located in the first few monolayers of the OSC on top of the dielectric surface. It is generally believed that the Frank–van der Merwe growth mode of organic thin films can provide better grain connectivity and thus carrier mobility.[6–8] Other than controlling the exposure environment, the utilization of self-assembled monolayers (SAMs) with different terminal groups on the dielectrics is also another popular approach to improve the quality of this interface.[9–15] The SAMs deposited onto dielectrics can be used to tune the surface energy and reduce the charge trap densities of the interface. However, the density and the alignments of the deposited SAM may vary between different processing approaches, and crystallized and well-oriented SAMs are required for a semiconductor to form densely packed film which is critical for OFET devices with high carrier mobility.[16,17] Usually, SAM deposition methods can be mainly classified into dry vapor phase[11,14,18,19] and solution depositions.[20,21] Among these two

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kinds of deposition methods, the former may be more prone to misalignment or the disorder of SAMs, and more importantly, more SAM molecules are wasted in comparison to the solution method. The most commonly used solution method is immersion, in which the substrates are immersed into SAM solutions for different time scales that range from an hour to tens of hours.[22,23] The self-assembly of SAMs on dielectric material is affected by a number of factors, such as alkyl chain length of the molecules,[24] deposition temperature,[17] and solvents used.[25] Although immersion would not waste SAM molecules like in the case of vapor deposition, the SAMs deposited by immersion usually cover the entire area of a dielectric, and confinement of the SAMs to certain regions would often require extra etching or patterning steps. This is also the case for other solution methods, such as the Langmuir–Blodgett (LB)[26] or spin-coating method.[27–29] Although the deposition time or complexity of the fabrication process may not be the first priority for devices in the laboratory, they are critical in the mass production of organic electronics where many devices with a variety of functions are required to be fabricated together onto the substrate and thus direct patterning of SAMs is highly desired especially for the development of organic complementary metal-oxide semiconductors (CMOS). As a result, there is a strong demand to develop a direct patterning method of SAMs which can functionalize different locations of a substrate for the large area toward the mass production of organic electronic components and ultimately CMOS circuits. Currently, one way to adjust the dielectric surface energy for the growth of p-type and n-type OSCs in CMOS organic inverters is by mixing two types of SAMs with specific molar ratios and depositing them together; however, since the mixed SAM is unpatterned, the threshold voltage of individual p-type or n-type transistors and the growth mode of different semiconductors cannot be independently adjusted which limits the optimization of the inverter gain. In order to directly pattern the deposited SAMs, the microcontact printing (μCP) method has been adapted previously, which used polydimethylsiloxane (PDMS) stamps to pattern the SAMs down to a submicrometer scale for device fabrications.[30–32] However, the transferred SAM layers by using PDMS stamping are usually less ordered than the solution deposited SAMs and result in OFETs that suffer from larger leakage currents and restrict their application in the mass manufacturing of organic electronics. As a consequence, a universal, directly patternable, and time-saving deposition method for SAMs onto different dielectric surfaces is highly desired but remains to be found. Combining such a SAM patterning method with other semiconductor processing approaches for large areas, such as vapor-jet printing, ink-jet printing or roll-to-roll deposition, the mass production of large scale organic electronic components and circuits would be feasible, which is an important step toward the commercialization of organic electronics.

Here, we introduce a new direct patterning method of SAMs by stamping and roller printing with a special designed hydrocarbon paraffin stamp. The paraffin wax, which consists of hydrocarbon molecules with different chain lengths (general formula C_nH_{2n+2}, $n = 17–35$), is melted and shaped by different molds developed by using a 3D printer. Various patterns can also be developed onto the mold by the 3D printer. The paraffin stamp that we developed is used to pick up SAMs in a solvent and directly transfer them onto a dielectric surface. In the SAM molecules, the anchor (head) group is specially designed to bond to particular dielectric materials or metals such as —$SiCl_3$ group in organosilanes for attaching onto silicon dioxide (SiO_2), —$PO(OH)_2$ group in phosphonic acids for bonding to metal oxide surfaces, or thiols (—S—H) for metal electrodes treatment for bottom contact devices.[33] On the other hand, a number of commonly used SAMs (e.g. octadecyltrichlorosilane (OTS), octadecylphosphonic acid (ODPA), tetradecylphosphonic acid (TDPA), and 1-dodecanethiol (1DT)) have alkyl chains as the terminal (tail) groups. The similar chemical structure of the paraffin hydrocarbon and the tail group of SAMs has allowed us to use their attractive van der Waals force for the direct patterning of SAMs. During the printing, the tail groups of the SAMs are attracted to the paraffin wax molecules, and the hydrophilic anchor groups tend to escape and aggregate on the interface of the dielectric and hydrocarbon layers. Since SAM has been directly arranged during the transfer by using the stamp, instead of slowly diffusing onto the dielectric as an immersion method, it only takes several minutes for SAM molecules to be patterned with good direction. Although post-processing treatments on the SAM and dielectric interface are needed, generally the required time is still shorter than immersion method. SAMs with end groups other than alkyl chains can also be deposited by this method by modifying the chemical components of the paraffin. Here, we apply this printing method by using a paraffin stamp to deposit OTS and trichloro (1H,1H,2H,2H-perfluorooctyl) silane (C8-PFTS) onto SiO_2, OPDA, and 1H,1H,2H,2H-perfluorooctanephosphonic acid (C8-PFPA) onto aluminum oxide (AlO_x) to modify the dielectric surface energy for the growth of dinaphtho[2,3-b:2′,3′-f]thieno[3,2-b]thiophene (DNTT, p-type) and copper(II) 1,2,3,4,8,9,10,11,15,16,17,18,22,23,24,25-hexadecafluoro-29H,31H-phthalocyanine (F_{16}CuPc, n-type) overlying the OSC layers. The DNTT and F_{16}CuPc transistors show a maximum carrier mobility of 3.02 and 0.018 $cm^2\ V^{-1}\ s^{-1}$ respectively, which is comparable with the state-of-art values of these two types of OSCs. We increase the scale of the approach further in terms of a roller imprint for a larger area of the Si/SiO_2 substrate and test the uniformity of an array of 16 × 16 transistors. Among these 256 devices, almost all of them showed similar transfer curves and the overall yield rate of the OFETs developed by this method is higher than 99%. Besides, we also pattern different SAMs onto glass substrates to demonstrate high gain CMOS inverters with AlO_x dielectric. Our current SAM deposition method can potentially be applied to the patterning of large areas and mass production of high performance organic electronic devices and components.

2. Results and Discussion

The schematic processing diagrams of the proposed stamping method of SAMs is presented in **Figure 1**. The direct printing stamps or roller stamps are made by melting refined paraffin wax at a temperature of 80 °C and then the paraffin is solidified in a polylactic acid (PLA) mold developed by a 3D printer with predefined features, such as step and trough. The stamp

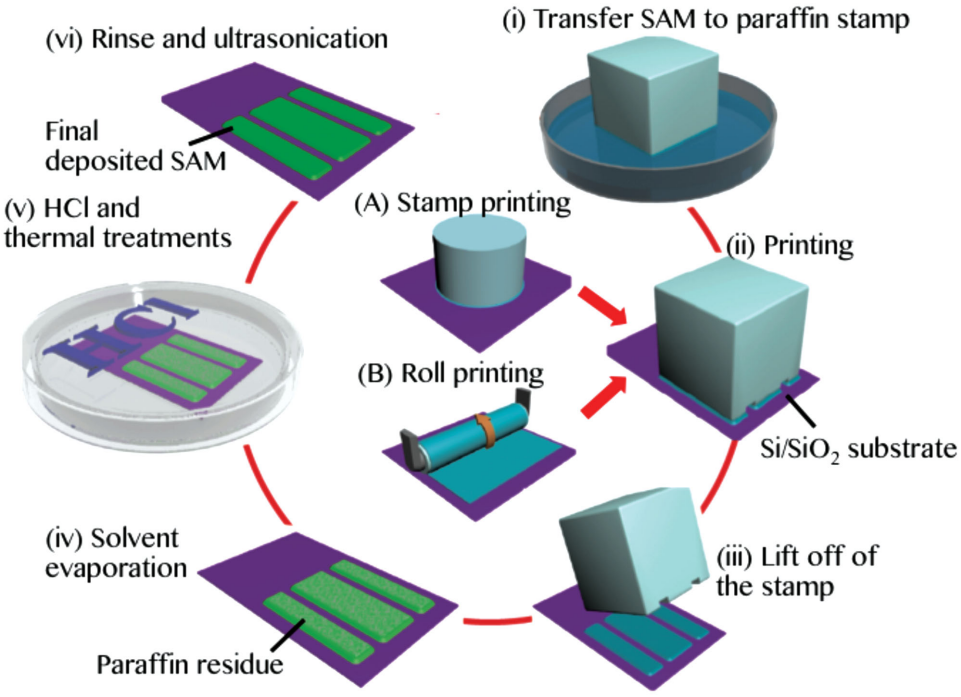

Figure 1. Stamp printing process of SAM.

with patterned features is immersed into the SAM solution for 3 min, and then the stamp is used to print onto the desired region of the substrates under careful alignment. Besides the mass of the stamp (20 g), no extra force is applied onto the stamp during the imprinting process. As the hydrophobic alkyl chains are attracted to the paraffin, whereas the hydrophilic anchor groups would be attached to the high energy surface of the substrate, the SAM molecules are able to stand up on the surface of the substrate. Similar for large area substrates, the roller stamp with the SAM solution is rolled on top of the substrates to perform printing under a constant loading of ≈2 N and a horizontal speed of 5 mm s^{-1}. The printed SAMs are then vapor treated with hydrochloric acid (HCl) and thermally annealed under vacuum to remove unwanted solvents and residues (HCl was used in order to accelerate the hydrolysis thus forming bond between silanes and silicon substrate[28]). To ensure that the printed SAMs are monolayers, the sample is ultrasonicated in various solvents (hexane, acetone, 2-propanol) for 20 min. After the SAM treatment, 30 nm DNTT and 50 nm silver source/drain electrodes are thermally evaporated through shadow masks under 10^{-6} Torr and room temperature to complete the OFET device.

To verify the quality of the SAMs, it is important to compare the properties of the printed SAMs with those obtained by the conventional immersion method and the results are summarized in **Figure 2**. Figure 2a,b show the atomic force microscopy (AFM) images of the stamp deposited and immersion deposited OTS on SiO_2, respectively. It can be noticed that from the stamping method, a uniform layer of SAM is formed without obvious defective points over the whole scanning area, and the root mean square (RMS) roughness of the layer is 0.22 nm. On the other hand, for the OTS monolayer deposited by the immersion method (18 h, 60% humidity), irregular spots with high levels of roughness can be clearly observed in the AFM images in Figure 2b. The measured height of these peaks exceeds 10 nm, which suggests that these are aggregations rather than multilayers of OTS. A similar phenomenon is observed in the immersed OTS also and have been reported in the work of others.[34,35] The irregular spots formed by aggregation and polymerization of the OTS molecules in the solvent are unavoidable in the immersion method which requires long processing time. However, for the fast method of stamping, since the deposition process is in terms of minutes thus it can significantly suppress the polymerization process, thus the sample has a roughness similar to the bare SiO_2 surface.

The crystallinity and ordering of the stamped SAMs are confirmed by using attenuated total reflectance Fourier transform infrared (ATR-FTIR) spectroscopy, X-ray reflectivity (XRR), and in-plane X-ray diffraction (XRD) measurements. The peak positions of the asymmetric stretching vibration of the methyl (—CH_3), and methylene (—CH_2—) groups of highly ordered crystalline SAMs in the IR spectrum are located at 2956 and 2851 cm^{-1}, respectively, while the symmetric stretching of —CH_2— is at 2918 cm^{-1} (accurate within 1 cm^{-1}).[26,36] A comparison between the ATR-FTIR results of the stamped SAMs with these values provided qualitative characterization of the crystallinity of the SAMs and positive shifts of these peaks would occur on the less ordered molecular assemblies. It can be seen from Figure 2c that the peaks for the stamp deposited OTS monolayers are 2851, 2919, and 2955 cm^{-1}, which are very close to the highly ordered crystalline values, similar to the SAMs deposited by the immersion method. The ATR-FTIR results confirm that the stamping process can provide a

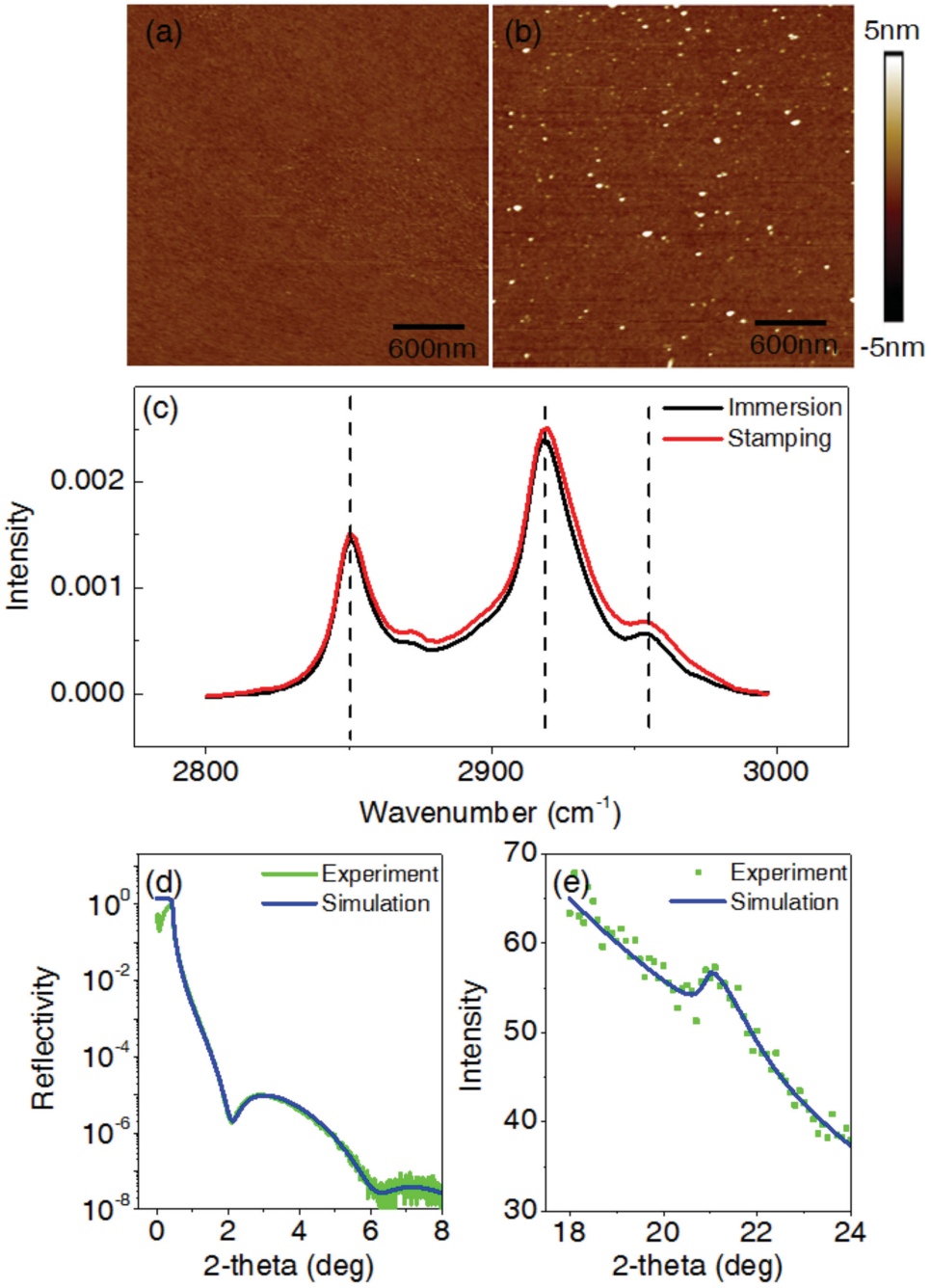

Figure 2. AFM morphology images of OTS monolayer deposited by a) stamping method, RMS roughness equals 0.22 nm and b) immersion method, RMS roughness of 0.96 nm. c) ATR-FTIR spectrum of OTS monolayers deposited by immersion and stamping methods, both show crystallized structure. d) XRR of stamped OTS layer which indicates thickness of 2.14 nm. e) In-plain XRD spectrum of stamped OTS with peak position at 21.13 ° and lattice constant of 4.2 Å.

highly crystallized layer of SAM. Here, we further employ XRR and in-plane XRD to measure the thickness and in-plane lattice constant of the highly ordered SAMs. From the XRR spectrum shown in Figure 2d, the height of the stamp printed SAM is estimated to be 2.14 nm which corresponds to an inclined angle of 21.5° normal to the dielectric surface given that the molecular length of the OTS is 2.3 nm. Furthermore, the in-plane XRD spectrum (Figure 2e) indicates that the highly ordered SAM has a lattice constant of 4.2 Å, which is very similar to the layer formed by the LB (50 mN m^{-1}) or spin-coating method.[26,28]

After investigating the intrinsic properties of the SAM deposited by stamp printing, we proceed a step further to apply SAMs in OFETs. The schematic diagram of the bottom gate, top source—drain contact OFETs is shown in **Figure 3**a. Here, we have three devices including: (i) bare SiO_2 surface, (ii) OTS

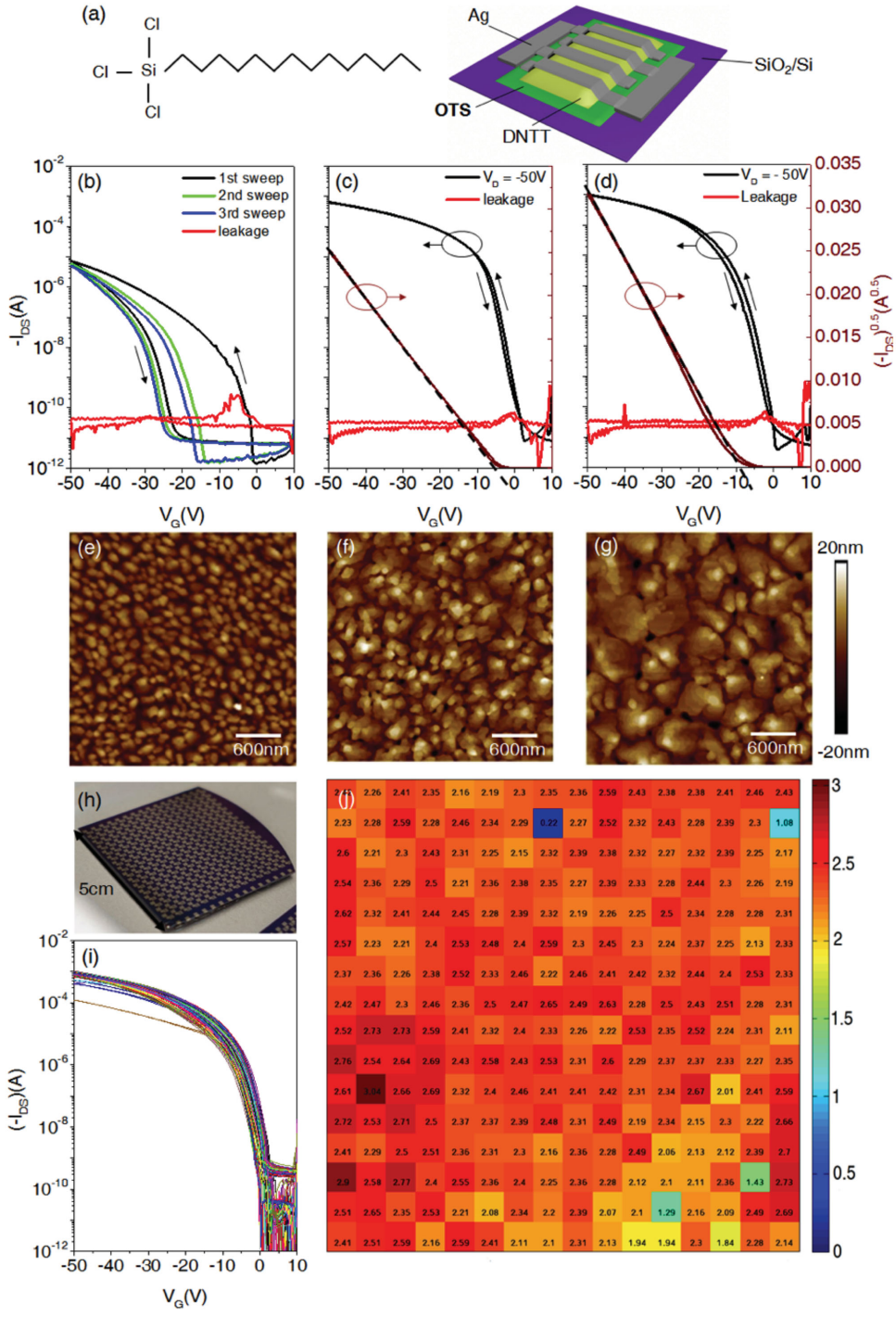

Figure 3. a) Molecular structure of OTS and schematic of DNTT based OFETs, $W/L = 40$. b–d) Transfer curves of OFETs fabricated on b) bare SiO_2 (μ_{av} = 0.17 $cm^2 V^{-1} s^{-1}$), c) immersion deposited OTS (μ_{av} = 1.44 $cm^2 V^{-1} s^{-1}$), and d) stamp printed OTS (μ_{av} = 2.72 $cm^2 V^{-1} s^{-1}$). e–g) AFM images of 30 nm thick DNTT evaporated on e) bare SiO_2/Si surface, f) immersion deposited OTS, and g) stamp printed OTS. h) View of array of 16 × 16 transistors with a large area on stamp printed OTS/SiO_2/Si. i) Transfer curves of all 256 devices with good uniformity, average mobility is around 2.4 $cm^2 V^{-1} s^{-1}$. j) Mobility distribution, there are only 4 malfunctioning devices with mobility lower than 2 $cm^2 V^{-1} s^{-1}$.

treated SiO_2 by immersion, and (iii) stamp printed OTS for direct performance comparison, and all tests are carried out in a glove box filled with nitrogen gas. The corresponding transfer curves of these three kinds of devices are shown in Figure 3b–d and the average carrier mobility of DNTT is 0.17, 1.44, and 2.72 $cm^2 V^{-1} s^{-1}$ respectively. The highest mobility of the devices with immersed and stamped SAMs is 1.70 and 3.02 $cm^2 V^{-1} s^{-1}$ respectively (see Figure S2 in the Supporting

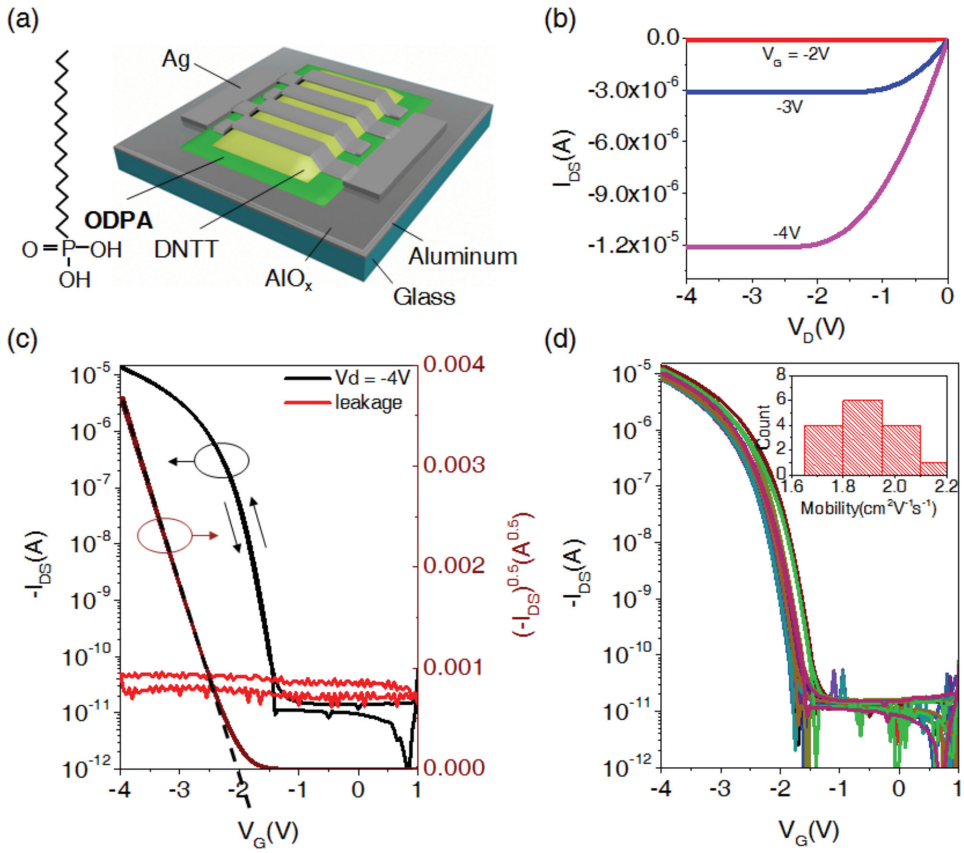

Figure 4. a) ODPA molecular structure and OFET fabricated by using paraffin to stamp ODPA onto AlO_x/Al/glass ($W/L = 20$). b) Output and c) transfer curves of transistor based on DNTT. d) Transfer curves of all 15 OFETs and their mobility histogram, average mobility is 1.9 $cm^2\ V^{-1}\ s^{-1}$ and highest can reach 2.11 $cm^2\ V^{-1}\ s^{-1}$.

Information for the transfer curves of all 15 devices). From the AFM morphology images of the DNTT at the channel region (Figure 3e–g), it could be observed that DNTT grown on a bare SiO_2 surface shows an average grain size of 120 nm only, which is significantly smaller than that of the DNTT grown on immersion or stamp deposited SAMs. DNTT grains on stamped OTS have a larger grain size and less grain boundary density. Other than lower carrier mobility, the devices with a bare SiO_2 dielectric layer also show a hysteresis effect, which could be due to the presence of charge trapping sites, such as —OH bonds on the surface of the SiO_2 which can be significantly suppressed by the SAMs.[37] For devices with immersion deposited SAMs, it is worth noting that the average mobility (1.44 $cm^2\ V^{-1}\ s^{-1}$), threshold voltage (−5 V), and on/off ratio (10^8) of our immersion deposited sample are actually very similar to the values reported in the literature.[38] Furthermore, for the samples with a stamp printed OTS layer, the higher mobility is even comparable to that of DNTT deposited onto a substrate at 60 °C (optimal temperature for vacuum deposited thin films of DNTT that have the highest mobility).[38–40] These findings allow us to benchmark the effectiveness of our method that uses paraffin in stamping and directly prove its potential application in the fabrication of organic electronic devices. In order to further clarify the function of paraffin stamping in the deposition of SAMs, we also used a control, by using the same treatment procedure on the SAMs without the paraffin stamp but instead just dropped 20 µL of SAM solution onto the substrate and undergoing the same vapor phase treatment with HCl, thermal annealing, and ultrasonication. The devices only show a carrier mobility of 1.1 $cm^2\ V^{-1}\ s^{-1}$ (Figure S3, Supporting Information).

With demonstrated success on small substrate devices, we proceeded to use the printing method with the paraffin stamp to fabricate an array of 16 × 16 transistors on a 2 × 2 in. Si/SiO_2 substrate in order to show the compatibility of the paraffin stamp with the rolling deposition technique. Among all the printing technologies for large area, such as gravure printing, screen printing, inkjet printing, blade coating, and slot die coating,[41–48] gravure printing could be directly applied to our method by molding the stamps into cylindrical shape for direct printing. The gravure printing technology is not only for scaling up the deposition of the SAMs but also allow us to pattern the SAM directly and make it compatible for the next stage of active layer deposition. The optical image of the transistor array is shown in Figure 3h and the corresponding transfer curves and carrier mobility of distribution are plotted in Figure 3i,j, respectively. In these 256 devices, only four of them show carrier mobility less than 1.5 $cm^2\ V^{-1}\ s^{-1}$ and only one device has a mobility less than 1 $cm^2\ V^{-1}\ s^{-1}$. These numbers correspond to a yield rate of around 98.5% and 99.5%, respectively. The uniform mobility color map (average mobility of 2.4 $cm^2\ V^{-1}\ s^{-1}$,

maximum of 3.04 cm^2 V^{-1} s^{-1}) clearly demonstrates the capability of the currently proposed printing method with a paraffin stamp for roll-to-roll deposition of SAMs onto large areas.

Although the thermally grown SiO_2 has a smooth surface for the deposition of SAMs, the low dielectric constant value of SiO_2 (ε_{SiO2} = 3.9) requires a large gate bias voltage which places limitations on the OFETs in portable device applications. Here, we further combined paraffin stamp printing with galvanic anodization to print ODPA onto anodized AlO_x, a high-k dielectric, to develop OFETs that have low operating power. The electrolytes, pH values, current density, voltage, and other parameters are carefully controlled and monitored in the anodization process (see the Experimental Section for details). By using a metal–insulator–metal (MIM) structure, the areal capacitance of the ODPA on AlO_x is 180 nF cm^{-2} (34 nm anodized AlO_x/ODPA) and around a fifteen fold increase in comparison to the OTS deposited onto 11.5 nF cm^{-2} of SiO_2 (300 nm of SiO_2/OTS). The significant increase in the dielectric capacitance allows us to operate the OFETs at much lower voltages and **Figure 4** shows a typical transfer curve of the DNTT OFETs fabricated on AlO_x with stamp printed ODPA. The average carrier mobility is 1.9 cm^2 V^{-1} s^{-1} (highest 2.11 cm^2 V^{-1} s^{-1}), on/off ratio is 10^6, and threshold voltage is −1.94 V. Similar to the OTS devices, the stamp printed samples show better device performance than that of the immersion samples (Figure S4, Supporting Information). The devices fabricated on AlO_x show lower carrier mobility than the one fabricated on SiO_2 which may be attributed to three major reasons: (i) higher surface roughness on the anodized AlO_x (RMS roughness: 0.84 nm, see Figure S5 in the Supporting Information),[49,50] (ii) carrier localization due to increasing dielectric polarizability,[51,52] and (iii) stronger contact resistance effect when the drain–source voltage V_{DS} is reduced due to the usage of high-k dielectric insulator.

So far, both of the SAMs that we used (OTS and ODPA) contained alkyl chains as the tail group which is suitable for the thermal evaporation growth of commonly used OSCs, such as pentacene and DNTT. However, their effects on other n-type semiconductors may not be as optimized and other kinds of SAMs with fluoroalkyl chains are usually used to reduce the trap densities and adjust the threshold voltages. This is particularly important for the complementary circuits that are integrated with p-channel and n-channel transistors.[31,40,53] Since previous paraffin wax is not suitable to print the SAMs with the tail groups of fluoroalkyl chains, we further modify the contents of the paraffin wax by blending with micronized polytetrafluoroethylene (PTFE)-modified polyethylene wax (see Figure S6, Supporting Information). C8-PFTS was printed onto SiO2, and C8-PFPA was used onto AlO_x respectively. **Figure 5** shows the transfer curves of the n-type $F_{16}CuPc$ OFETs on both substrates and these devices have a similar mobility around 0.0125 cm^2 V^{-1} s^{-1} with a positive threshold voltage of 19 and 2.1 V, respectively. By showing these highly comparable transfer curves with one that has been reported,[10] it is obvious that the current SAM deposition method could be used for different kinds of SAMs with different terminal groups, and a very competitive performance can be achieved by such a time saving direct patterning method of SAMs. The performances of the OFETs mentioned above are summarized in **Table 1**.

One of the major objectives of this study is to employ the stamping method to print and pattern different SAMs onto various regions of a dielectric surface and then fabricate CMOS-inverters that have low operating voltage based on such. CMOS inverters, also known as NOT logic gates, are widely used

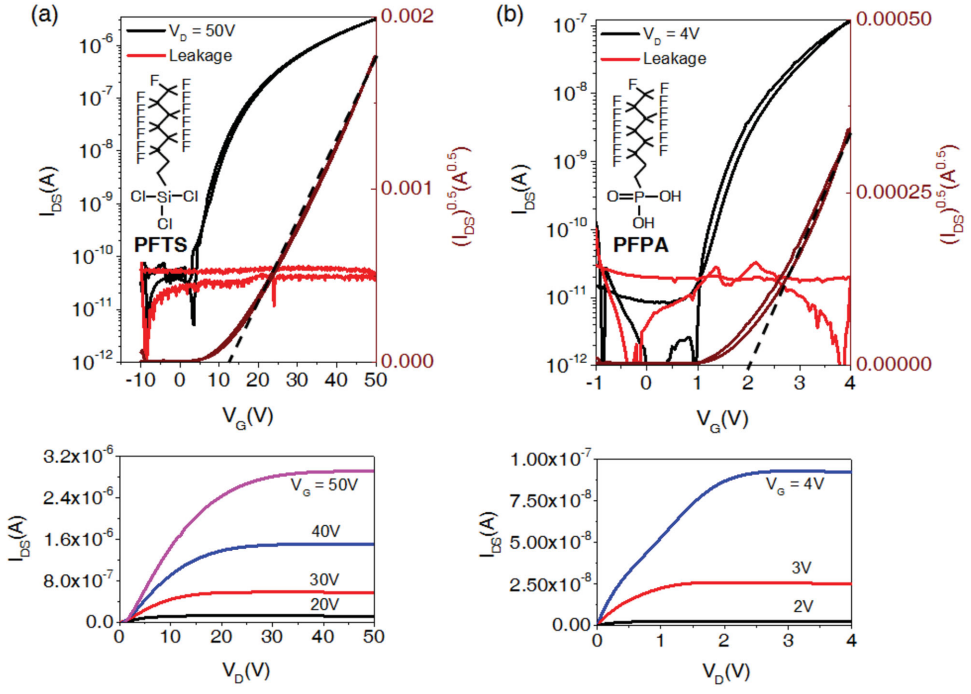

Figure 5. *I–V* and output curves of OFETs based on $F_{16}CuPc$ fabricated on a) C8-PFTS/SiO_2/Si substrate and b) C8-PFPA/AlO_x/Al/glass.

Table 1. Characterization of OFETs.

	DNTT				F_{16}CuPc	
	Stamp OTS	Immersion OTS	Stamp ODPA	Immersion ODPA	Stamp C8-PFTS	Stamp C8-PFPA
W/L	40	40	20	20	40	20
μ_{ave} (μ_{max}) [$cm^2\ V^{-1}\ s^{-1}$]	2.75(3.02)	1.44(1.70)	1.90(2.11)	1.29(1.62)	0.0126 (0.0180)	0.0128 (0.0175)
V_{th} [V]	−9	−5.0	−1.9	−1.9	19.0	2.1
I_{on}/I_{off}	2×10^8	10^8	10^6	3.3×10^5	10^5	10^4

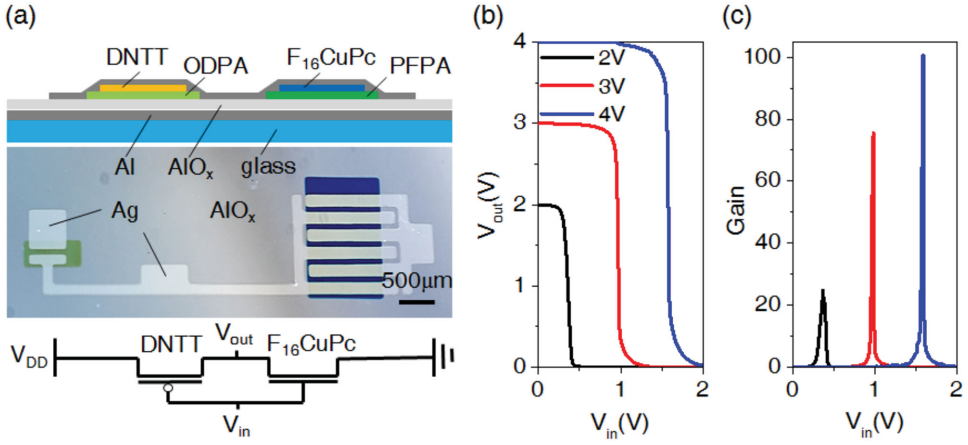

Figure 6. Complementary inverter which consists of p-channel and n-channel OFETs on different SAMs deposited by stamping method. a) Schematic and photo of the inverter, on anodized AlO_x dielectric surface. ODPA was stamped on the region of p-type DNTT transistor and PFPA was stamped onto the region of n-type F_{16}CuPc transistor, than semiconductors and source/drain electrodes are deposited separately by thermal evaporation through shadow masks. Input voltage (V_{in}) was added to the gate electrode and output voltage (V_{out}) was measured at the connection electrode of 2 transistors. b) Transfer curves of V_{out} varying with V_{in}, supply voltage V_{DD} = 2–4 V. c) Gain values of the inverter.

in digital logic circuits for logic functions due to their high switching speed, low power consumption, and robustness to noise. CMOS inverters consist of both p-type and n-type transistors and the threshold voltages of these two types of transistors should be carefully tuned to achieve high inverter gain and noise margin (NM). However, for CMOS inverters based on OFETs, the direct patterning of SAMs onto a single substrate by using existing solutions or vapor deposition methods remains challenging, and mixed SAMs are usually applied and the threshold voltages of the transistors are modified together as a whole.[10] The major drawback of mixed SAMs is the lack of flexibility in independently tuning the performance of the p-type and n-type transistors. Here, by applying the proposed stamping method, we can pattern different types of SAMs and separately adjust the performances of the p-channel and n-channel OFETs. The schematics and transfer characteristics of the complementary circuits on an AlO_x dielectric are shown in **Figure 6**. We utilize DNTT and F_{16}CuPc as the active layer materials and ODPA and C8-PFPA are separately printed on the dielectric. Both OFETs in a complementary inverter have a channel length of 100 μm, while the channel width for the p-type transistor is 500 μm and for the n-type transistor is 7500 μm. The inverter is operated with a supply voltage V_{DD} that ranges from 2 to 4 V added to the source of the p-type transistor, and the voltage gain reaches 102 when the V_{DD} is equal to 4 V. Another important performance indicator of inverters is the NM, which indicates the noise immunity of a device, i.e., the maximum noise signal that will not cause the malfunction of inverters. NM at high level (NM_H) and low level (NM_L) should be larger than 10% of the 0.5 V_{DD} and are evaluated by the highest and lowest input voltages (V_{IH}, V_{IL}) and the highest and lowest output voltages (V_{OH}, V_{OL})[54]

$$\begin{cases} \mathrm{NM}_H = V_{OH} - V_{IH} \\ \mathrm{NM}_L = V_{IL} - V_{OL} \end{cases} \quad (1)$$

when V_{DD} equals to 4 V, NM_H and NM_L are 2.4 and 1.4 V, respectively, which is high enough for inverters to withstand noises under different bias conditions and such an organic CMOS inverter is already suitable for applications in more advanced logic gates or circuits.

3. Conclusion

In summary, we have explored a new way to deposit SAMs which could easily be patterned onto different dielectric surfaces by direct printing. The results provide compelling

evidences that this approach has significant advantages over the conventional SAMs developed by using vapor or solution deposition. The proposed stamp or roller printing method can significantly reduce the deposition time and compatible with the roll-to-roll fabrication of large areas. The organic transistors developed on these dielectric insulators usually show better performance than the devices with SAMs developed by using immersion method. The uniform and densely packed SAMs have been examined by using the water contact angle, and through AFM, XRD, and ATR-FTIR characterizations. By modifying the chemical composition of the paraffin stamp, different SAMs including those made of OTS, ODPA, C8-PFTS, and C8-PFPA, have been directly printed onto the dielectric. Complementary inverters with patterned dielectrics developed by using this printing method show a gain higher than 100. We believe the current SAM printing method can be further applied to solution processing OFETs by using a suitable stamp to print other SAMs with strong wettability. This universal and direct SAM printing method reported in the current work is suitable for implementation in high performance organic circuits with a large area and also in mass production.

4. Experimental Section

Materials: The SAMs were purchased from Sigma-Aldrich without further purification. OTS was stored in a nitrogen atmosphere at room temperature (RT). 2-propanol, hexane, acetone, and other solvents were bought from Advanced Technology & Industrial Co., Ltd. and used directly. Silicon wafers with 300 nm of thermally grown silicon oxide came from Silicon Quest International. DNTT and $F_{16}CuPc$ were obtained from Luminescence Technology Corporation and both were used as received.

SAM Treatment: A 10×10^{-3} M solution of OTS in 2-propanol was prepared in a glove box with nitrogen (99.999% pure) and then stamped onto a designated region of the Si/SiO_2 substrate for 20 s without additional force to transfer the SAM solution (for high-k AlO_x, 5×10^{-3} M of ODPA in 2-propanol was used). After repeating the stamping procedure two to three times, the samples were left for several minutes in air until the solvent evaporated. Since a small amount of hydrocarbon molecules were dissolved into the solvent, the paraffin molecules continued to help to position the SAMs during the solvent evaporation and vapor annealing process. After the solvent evaporated, the samples were placed under a HCl vapor environment for 2 h (for ODPA fabricated onto AlO_x, no HCl treatment was applied) to make sure the SAM molecules have been bonded to dielectric surfaces. Then the samples were annealed at 120 °C in a vacuum oven for 40 min in order to remove the residual solvents and HCl. For the practical roll-to-roll manufacturing process, the post-processing annealing time of the SAM could be further optimized with the deposition of other active layers and electrodes which also need high temperature treatments. Finally, the samples were cleaned and SAM multilayers were removed through ultrasonication in hexane for 10 min, acetone for 5 min and 2-propanol for 5 min, respectively. The annealing process has several functions: first, it helps with the formation of chemical bonds between the substrate and SAM molecules; second, the annealing process can also help to remove paraffin wax residues, since the heat may reduce the van der Waals forces between the hydrocarbon and SAM molecules, residues can be easily removed with a hexane rinse. For comparison purposes, we used the immersion method and simply immersed the cleaned silicon substrate with silicon oxide into 5×10^{-3} M hexane solution of OTS or glass substrate with AlO_x into 2×10^{-3} M 2-propanol solution of ODPA for 18 h at room temperature, and then cleaned by using ultrasonication.

Aluminum Anodization: Aluminum (100 nm) was used to make the gate electrode, and thermally evaporated at 10 nm s^{-1} onto the glass substrates in a thermal evaporation chamber without a shadow mask. Then the aluminum was anodized in electrolyte that contained citric acid and sodium citrate dissolved in deionized water (pH ≈ 7). The anodization process comprised two stages: galvanostatic and potentiostatic anodizations. The constant current was set as 0.7 mA cm^{-2}. The thickness of the AlO_x was increased as the anodization voltage increased, approximately 1.6 nm V^{-1},[55] and the final thickness of the AlO_x ($1.6 \times 2 + 2 = 34$ nm, plus 2 nm normally grown AlO_x) is dependent on the voltage limit, which is 20 V in this study. Anodization was finished within 3 min when the current dropped to 10% of the initial constant current and the surface roughness of the formed AlO_x was 0.84 nm.

Fabrication of OFET Device: Silicon substrate with 300 nm silicon oxide or glass substrate with Al/AlO_x was cleaned by using ultrasonication, then treated with an oxygen plasma cleaner (Harrick Scientific, PDC-001, 30 W) for 15 min. After the cleaning of the substrates, the SAMs were deposited by using the above methods. DNTT (30 nm) was thermally evaporated through a shadow mask at 0.3 Å s^{-1} onto the substrates by using an evaporation chamber. The substrates were maintained at room temperature and pressure was maintained at 10^{-6} torr during the deposition. Then 50 nm of a silver source and drain electrodes were evaporated at 1 Å s^{-1} over the active layer through another shadow mask, in which the channel width and length were 4000 and 100 μm ($W/L = 40$) for the silicon substrates, and 2000 and 100 μm ($W/L = 20$) for the glass substrates, respectively.

Inverter Fabrication: The complementary inverters were fabricated onto the glass substrates with anodized AlO_x. Two kinds of SAMs were used for the inverter, which consisted of two transistors: ODPA was stamped onto the region of a p-type DNTT based transistor, and C8-PFPA for an n-type transistor with $F_{16}CuPc$ as the semiconductor. For C8-PFPA, we used paraffin wax blended with fluoride to make the stamps and the stamping procedure was the same as that for the ODPA. Then DNTT and $F_{16}CuPc$ were deposited by thermal evaporation respectively through different shadow masks and then the silver source and drain electrodes. All of the thermal evaporations were carried out under 10^{-6} Torr and room temperature.

Characterization: The water contact angle was tested by using a contact angle goniometer, Sindatek Model 100SB. Five points on each sample were measured, and the average value was taken as the final value. The surface energy was calculated by using the Owens–Wendt model.

The surface morphology was measured by using an AFM system, MultiMode 8 from Bruker. All images were taken in the probe tapping mode in air.

The ATR-FTIR spectrum was obtained by using the Bruker Tensor 27 FTIR spectrometer at the Chinese University of Hong Kong. A spectrum with a resolution of 4 cm^{-1} was obtained by subtracting the silicon wafer background signal from the signal of the SAM modified substrate.

XRR and in-plain XRD were carried out in the Application Laboratories of the Rigaku Corporation, Tokyo.

The electrical characteristics of the field-effect transistors were tested by using a Keithley 2636 dual-channel source meter under the sweeping mode in a glove box with nitrogen. The charge carrier mobility in the saturation regime was obtained from transfer curves by using the following equation

$$I_{ds} = \frac{W}{2L}\mu C_i (V_G - V_{th})^2 \quad (2)$$

where I_{DS} is the drain–source current, W and L indicate the channel width and length, respectively, μ is the desired mobility, $V_G - V_{th}$ refers to the difference between the gate and threshold voltages, C_i is the capacitance of the dielectric layer, which was tested by making a MIM structure and measured by using an LCR meter.

Supporting Information

Supporting Information is available from the Wiley Online Library or from the author.

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[1] K. M. Knesting, P. J. Hotchkiss, B. A. MacLeod, S. R. Marder, D. S. Ginger, *Adv. Mater.* **2012**, *24*, 642.
[2] M. Dubey, T. Weidner, L. J. Gamble, D. G. Castner, *Langmuir* **2010**, *26*, 14747.
[3] T. Sekitani, U. Zschieschang, H. Klauk, T. Someya, *Nat. Mater.* **2010**, *9*, 1015.
[4] M. Kaltenbrunner, T. Sekitani, J. Reeder, T. Yokota, K. Kuribara, T. Tokuhara, M. Drack, R. Schwödiauer, I. Graz, S. Bauer-Gogonea, *Nature* **2013**, *499*, 458.
[5] Z. Wang, X. Ren, C. Fan, Y. H. Chang, H. Li, H. Chen, S. P. Feng, S. Shi, P. K. Chan, *Adv. Mater. Inter.* **2014**, *1*, 1300119.
[6] A. A. Virkar, S. Mannsfeld, Z. Bao, N. Stingelin, *Adv. Mater.* **2010**, *22*, 3857.
[7] S. Verlaak, S. Steudel, P. Heremans, D. Janssen, M. S. Deleuze, *Phys. Rev. B* **2003**, *68*, 195409.
[8] W. Shao, H. Dong, L. Jiang, W. Hu, *Chem. Sci.* **2011**, *2*, 590.
[9] D. O. Hutchins, T. Weidner, J. Baio, B. Polishak, O. Acton, N. Cernetic, H. Ma, A. K.-Y. Jen, *J. Mater. Chem. C* **2013**, *1*, 101.
[10] U. Zschieschang, F. Ante, M. Schlörholz, M. Schmidt, K. Kern, H. Klauk, *Adv. Mater.* **2010**, *22*, 4489.
[11] J. F. Martínez Hardigree, T. J. Dawidczyk, R. M. Ireland, G. L. Johns, B.-J. Jung, M. Nyman, R. Österbacka, N. Marković, H. E. Katz, *ACS Appl. Mater. Interfaces* **2013**, *5*, 7025.
[12] Y. M. Park, J. Daniel, M. Heeney, A. Salleo, *Adv. Mater.* **2011**, *23*, 971.
[13] D. Liu, X. Xu, Y. Su, Z. He, J. Xu, Q. Miao, *Angew. Chem. Int. Ed.* **2013**, *52*, 6222.
[14] S. Kobayashi, T. Nishikawa, T. Takenobu, S. Mori, T. Shimoda, T. Mitani, H. Shimotani, N. Yoshimoto, S. Ogawa, Y. Iwasa, *Nat. Mater.* **2004**, *3*, 317.
[15] U. Zschieschang, T. Yamamoto, K. Takimiya, H. Kuwabara, M. Ikeda, T. Sekitani, T. Someya, H. Klauk, *Adv. Mater.* **2011**, *23*, 654.
[16] S. R. Walter, J. Youn, J. D. Emery, S. Kewalramani, J. W. Hennek, M. J. Bedzyk, A. Facchetti, T. J. Marks, F. M. Geiger, *J. Am. Chem. Soc.* **2012**, *134*, 11726.
[17] H. S. Lee, D. H. Kim, J. H. Cho, M. Hwang, Y. Jang, K. Cho, *J. Am. Chem. Soc.* **2008**, *130*, 10556.
[18] S. Gupta, H. Gleskova, *Org. Electron.* **2013**, *14*, 354.
[19] J. Roh, C.-M. Kang, J. Kwak, C. Lee, B. J. Jung, *Appl. Phys. Lett.* **2014**, *104*, 173301.
[20] K. Kuribara, H. Wang, N. Uchiyama, K. Fukuda, T. Yokota, U. Zschieschang, C. Jaye, D. Fischer, H. Klauk, T. Yamamoto, *Nat. Commun.* **2012**, *3*, 723.
[21] O. Acton, D. Hutchins, L. Árnadóttir, T. Weidner, N. Cernetic, G. G. Ting, T. W. Kim, D. G. Castner, H. Ma, A. K. Y. Jen, *Adv. Mater.* **2011**, *23*, 1899.
[22] H. Klauk, U. Zschieschang, J. Pflaum, M. Halik, *Nature* **2007**, *445*, 745.
[23] N. Rozlosnik, M. C. Gerstenberg, N. B. Larsen, *Langmuir* **2003**, *19*, 1182.
[24] K. Fukuda, T. Hamamoto, T. Yokota, T. Sekitani, U. Zschieschang, H. Klauk, T. Someya, *Appl. Phys. Lett.* **2009**, *95*, 203301.
[25] Y.-A. Cheng, B. Zheng, P.-H. Chuang, S. Hsieh, *Langmuir* **2010**, *26*, 8256.
[26] A. Virkar, S. Mannsfeld, J. H. Oh, M. F. Toney, Y. H. Tan, G. Y. Liu, J. C. Scott, R. Miller, Z. Bao, *Adv. Funct. Mater.* **2009**, *19*, 1962.
[27] H.-Y. Nie, M. J. Walzak, N. S. McIntyre, *J. Phys. Chem. B* **2006**, *110*, 21101.
[28] Y. Ito, A. A. Virkar, S. Mannsfeld, J. H. Oh, M. Toney, J. Locklin, Z. Bao, *J. Am. Chem. Soc.* **2009**, *131*, 9396.
[29] O. Acton, M. Dubey, T. Weidner, K. M. O'Malley, T. W. Kim, G. G. Ting, D. Hutchins, J. Baio, T. C. Lovejoy, A. H. Gage, *Adv. Funct. Mater.* **2011**, *21*, 1476.
[30] U. Zschieschang, M. Halik, H. Klauk, *Langmuir* **2008**, *24*, 1665.
[31] I. Hirata, U. Zschieschang, F. Ante, T. Yokota, K. Kuribara, T. Yamamoto, K. Takimiya, M. Ikeda, H. Kuwabara, H. Klauk, *MRS Commun.* **2011**, *1*, 33.
[32] J. A. Rogers, Z. Bao, A. Makhija, P. Braun, *Adv. Mater.* **1999**, *11*, 741.
[33] W. H. Lee, J. H. Cho, K. Cho, *J. Mater. Chem.* **2010**, *20*, 2549.
[34] A. Y. Fadeev, T. J. McCarthy, *Langmuir* **2000**, *16*, 7268.
[35] H.-C. Tiao, Y.-J. Lee, Y.-S. Liu, S.-H. Lee, C.-H. Li, M.-Y. Kuo, *Org. Electron.* **2012**, *13*, 1004.
[36] M. D. Porter, T. B. Bright, D. L. Allara, C. E. Chidsey, *J. Am. Chem. Soc.* **1987**, *109*, 3559.
[37] L.-L. Chua, J. Zaumseil, J.-F. Chang, E. C.-W. Ou, P. K.-H. Ho, H. Sirringhaus, R. H. Friend, *Nature* **2005**, *434*, 194.
[38] T. Yamamoto, K. Takimiya, *J. Am. Chem. Soc.* **2007**, *129*, 2224.
[39] T. Yamamoto, S. Shinamura, E. Miyazaki, K. Takimiya, *Bull. Chem. Soc. Jpn.* **2010**, *83*, 120.
[40] U. Kraft, M. Sejfi , M. J. Kang, K. Takimiya, T. Zaki, F. Letzkus, J. N. Burghartz, E. Weber, H. Klauk, *Adv. Mater.* **2015**, *27*, 207.
[41] R. Søndergaard, M. Hösel, D. Angmo, T. T. Larsen-Olsen, F. C. Krebs, *Mater. Today* **2012**, *15*, 36.
[42] P. H. Lau, K. Takei, C. Wang, Y. Ju, J. Kim, Z. Yu, T. Takahashi, G. Cho, A. Javey, *Nano Lett.* **2013**, *13*, 3864.
[43] H. Kang, R. Kitsomboonloha, J. Jang, V. Subramanian, *Adv. Mater.* **2012**, *24*, 3065.
[44] B. Peng, X. Ren, Z. Wang, X. Wang, R. C. Roberts, P. K. Chan, *Sci. Rep.* **2014**, *4*, 6430.
[45] K. Fukuda, Y. Takeda, Y. Yoshimura, R. Shiwaku, L. T. Tran, T. Sekine, M. Mizukami, D. Kumaki, S. Tokito, *Nat. Commun.* **2014**, *5*, 4147.
[46] Y. Mei, M. A. Loth, M. Payne, W. Zhang, J. Smith, C. S. Day, S. R. Parkin, M. Heeney, I. McCulloch, T. D. Anthopoulos, *Adv. Mater.* **2013**, *25*, 4352.
[47] S. Park, G. Giri, L. Shaw, G. Pitner, J. Ha, J. H. Koo, X. Gu, J. Park, T. H. Lee, J. H. Nam, *Proc. Natl. Acad. Sci. USA* **2015**, *112*, 5561.
[48] H. Youn, T. Lee, L. J. Guo, *Energy Environ. Sci.* **2014**, *7*, 2764.
[49] S. Steudel, S. De Vusser, S. De Jonge, D. Janssen, S. Verlaak, J. Genoe, P. Heremans, *Appl. Phys. Lett.* **2004**, *85*, 4400.
[50] S. E. Fritz, T. W. Kelley, C. D. Frisbie, *J. Phys. Chem. B* **2005**, *109*, 10574.
[51] H. Tan, N. Mathews, T. Cahyadi, F. Zhu, S. Mhaisalkar, *Appl. Phys. Lett.* **2009**, *94*, 263303.
[52] I. Hulea, S. Fratini, H. Xie, C. Mulder, N. Iossad, G. Rastelli, S. Ciuchi, A. Morpurgo, *Nat. Mater.* **2006**, *5*, 982.
[53] U. Kraft, U. Zschieschang, F. Ante, D. Kälblein, C. Kamella, K. Amsharov, M. Jansen, K. Kern, E. Weber, H. Klauk, *J. Mater. Chem.* **2010**, *20*, 6416.
[54] K. J. Baeg, M. Caironi, Y. Y. Noh, *Adv. Mater.* **2013**, *25*, 4210.
[55] M. Kaltenbrunner, P. Stadler, R. Schwödiauer, A. W. Hassel, N. S. Sariciftci, S. Bauer, *Adv. Mater.* **2011**, *23*, 4892.